

## CLAIMS

What is claimed is:

- 1 1. A processor comprising:
  - 2 a voltage supply input port to receive a voltage at a first voltage level; and
  - 3 a cache to flush or maintain, depending on a power status signal, its
  - 4 contents upon entering a low power state in which the voltage is to be
  - 5 received at a second voltage level, the second voltage level being
  - 6 lower than the first voltage level.
- 1 2. The processor of claim 1, wherein the voltage supply input port is coupled to
  - 2 the cache to power the cache, and the second voltage level is less than twice
  - 3 an average threshold voltage of a majority of transistors of the processor.
- 1 3. The processor of claim 1, further comprising:
  - 2 a power status signal port to receive the power status signal from an
  - 3 external source; and
  - 4 a core to receive the power status signal and to flush or maintain the
  - 5 contents of the cache depending on the power status signal.
- 1 4. The processor of claim 1, further comprising a core to generate the power
  - 2 status signal and to flush or maintain the contents of the cache depending on
  - 3 the power status signal.

- 1 5. The processor of claim 1, further comprising:  
2 a core to execute instructions; and  
3 a phase locked loop to provide a clock signal to the core, the clock signal  
4 to be off during the low power state.
- 1 6. The processor of claim 1, wherein the cache is an L1 cache, an L2 cache, or  
2 both.
- 1 7. The processor of claim 1, wherein the cache is to flush its contents upon  
2 entering the low power state if the power status signal indicates that a system  
3 in which the processor resides is to be suspended.
- 1 8. The processor of claim 1, wherein the cache is to flush its contents upon  
2 entering the low power state if the power status signal indicates that power  
3 reduction associated with maintaining the contents of the cache upon  
4 entering the low power state is a lower priority than avoiding an increase in a  
5 soft error rate in the cache associated with reducing the voltage to the second  
6 voltage level.
- 1 9. The processor of claim 8, wherein the power status signal indicates that  
2 power reduction associated with maintaining the contents of the cache upon  
3 entering the low power state is a lower priority than avoiding an increase in a  
4 soft error rate in the cache associated with reducing the voltage to the second

5 voltage level if the power status signal indicates that the voltage is being  
6 provided by an electrical power outlet.

1 10. The processor of claim 1, wherein the cache is to maintain its contents upon  
2 entering the low power state if the power status signal indicates that power  
3 reduction associated with maintaining the contents of the cache upon  
4 entering the low power state is a higher priority than avoiding an increase in a  
5 soft error rate in the cache associated with reducing the voltage to the second  
6 voltage level.

1 11. The processor of claim 10, wherein the power status signal indicates that  
2 power reduction associated with maintaining the contents of the cache upon  
3 entering the low power state is a higher priority than avoiding an increase in a  
4 soft error rate in the cache associated with reducing the voltage to the second  
5 voltage level if the power status signal indicates that the voltage is being  
6 provided by a battery.

1 12. A computer system comprising:  
2 a voltage regulator to supply a voltage at a first voltage level and to supply  
3 the voltage at a lower second voltage level while in a low power state;  
4 a cache, to be powered by the voltage from the voltage regulator; and  
5 a power manager to send a first or second signal if power reduction  
6 associated with maintaining contents of the cache upon entering the

7 low power state is a lower or higher priority, respectively, than avoiding  
8 an increase in a soft error rate in the cache associated with the low  
9 power state.

1 13. The computer system of claim 12, wherein the cache is to flush or maintain  
2 its contents if the processor receives the first or second signal, respectively,  
3 upon entering the low power state.

1 14. The computer system of claim 13, further comprising a clock to provide a  
2 clock signal to a core of a processor containing the cache, the clock signal to  
3 the core to be off during the low power state.

1 15. The computer system of claim 13, wherein the second voltage level is less  
2 than twice an average threshold voltage of a majority of transistors of the  
3 cache.

1 16. The computer system of claim 12, wherein the second voltage level is less  
2 than twice an average threshold voltage of a majority of transistors of the  
3 cache.

1 17. A computer system comprising:  
2 a voltage regulator to supply a voltage;  
3 a clock to provide a clock signal; and

4 a processor to receive the clock signal and the voltage, the processor  
5 including a cache, the processor to flush or maintain, depending on a  
6 power status signal, contents of the cache upon entering a low power  
7 state in which the clock is off and the voltage is reduced.

1 18. The computer system of claim 17, wherein the voltage regulator is to supply  
2 the voltage at a voltage level that is less than twice an average threshold  
3 voltage of a majority of transistors of the cache during the low power state.

1 19. The computer system of claim 17, wherein the voltage regulator is to supply  
2 the voltage to the processor at a reduced voltage level during the low power  
3 state, and the cache is to flush its contents upon entering the low power state  
4 if the power status signal indicates that the computer system is to be  
5 suspended.

1 20. The computer system of claim 19, wherein the cache is to maintain its  
2 contents upon entering the low power state if the power status signal  
3 indicates that the voltage is being provided by a battery.

1 21. The computer system of claim 20, wherein the cache is to flush its contents  
2 upon entering the low power state if the power status signal indicates that the  
3 voltage is being provided by an electrical power outlet.

1 22. A method comprising:  
2 triggering a processor of a computer system to enter a low power state in  
3 which a voltage supplied to a cache of the processor is reduced and a  
4 clock supplied to the processor is off; and  
5 flushing or maintaining contents of the cache upon entering the low power  
6 state depending on a power status signal.

1 23. The method of claim 22, further comprising flushing the contents of the cache  
2 upon entering the low power state if the computer system is to be suspended

1 24. A machine-readable medium including machine-readable instructions that, if  
2 executed by a machine, cause the machine to perform the method of claim  
3 22.

1 25. A machine-readable medium including machine-readable instructions that, if  
2 executed by a machine, cause the machine to perform the method of claim  
3 23.